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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,495	09/24/2001	Hiroyuki Amishiro	50090-338	5812

7590 10/18/2002

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EXAMINER	
SUTTON, TIMOTHY J	
ART UNIT	**PAPER NUMBER**
2813	9

DATE MAILED: 10/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,495	AMISHIRO ET AL.	
	Examiner	Art Unit	
	Timothy J Sutton	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 21* is/are pending in the application.

4a) Of the above claim(s) *14-21* is/are withdrawn from consideration.

5)☒ Claim(s) *4-10, 12, and 21* is/are allowed.

6)☒ Claim(s) *1-3,11 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-2, 11, & 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Babcock et al. (U.S. P.G. Publication 2002/0033519).

Re claim 1, Babcock et al. discloses a semiconductor device having a plurality of resistor elements (figure 2c, items 60 & 70) formed on an insulating film in predetermined regions on a surface of a semiconductor substrate (figure 2c, items 10 & 20), the semiconductor device comprising active regions proximate to each of the resistor elements (active regions are located to the left and to the right of the STI).

Re claim 2, the insulating film is an element isolating film formed by shallow trench isolation (paragraph 0017).

Re claim 3, the plurality of resistor elements are arranged on the insulating film and the insulating film is located under the resistor elements are set to a predetermined width by the active regions (figure 2c, items 20, 60, & 70).

Re claim 11, the active regions extend close to lengthwise ends of the resistor elements, which are surrounded by the active regions (figure 2c-the active regions that are located to the left and to the right of the resistors extend ***close*** to the resistor elements that are surrounded by the active region).

Re claim 13, the resistor elements are formed by a layer-constituting gate electrodes of MOS transistors furnished outside said predetermined regions (figure 2c, items 80, 70, & 60).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Babcock et al. in view of Wolf (Silicon Processing for the VLSI Era, Volume 2-Process Integration).

As stated in paragraph 4, all of the limitations have been taught except for the teaching of the insulating film under said resistor elements is set to a predetermined width by said active regions.

Wolf teaches the formation of two active regions with a shallow trench region. The width of the insulating region is predetermined by the amount of space between the two active regions (see figures 2-32 & 2-33).

It would be obvious to one with ordinary skill in the art that a predetermined width of the isolating region is defined by the distance between the two active regions as taught by Wolf.

Allowable Subject Matter

5. Claims 4-10, 12, and 21 are allowed.

Re claim 4, the prior teaches a semiconductor having a plurality of resistor elements formed on an insulating film in predetermined regions on a surface of a semiconductor substrate, the semiconductor device comprising: active regions proximate to each of the resistor elements, where the plurality of resistor elements are arranged on the insulating film, the insulating film under the resistor elements is set to a predetermined width by the active regions. However the prior art fails to teach in combination with the other claimed limitations the predetermined width is defined by an amount of shift in resistance value of the resistor elements, the amount of shift being determined by the predetermined width.

Re claim 5, the prior art teaches a semiconductor having a plurality of resistor elements formed on an insulating film in predetermined regions on a surface of a semiconductor substrate, the semiconductor device comprising: active regions to each of the resistor. However the prior art does not teach or fairly suggest the regions include the active regions are furnished with dummy gate electrodes constituting the same layer as that of the resistor elements.

Response to Arguments

6. Applicant's arguments filed July 3, 2002 have been fully considered but they are not persuasive.

7. Applicants argue that the Examiner has not identified any specific disclosure in Babcock regarding the active regions. Applicant also argues that the active regions are not positioned proximate to each of the resistor elements.

Applicant is ignoring the expressed teachings of Babcock specifically Figure 2B. Referring to Figure 2B, items 50 (gate dielectric in paragraph 17) and 80 (transistor gate structure in paragraph 18) the regions therebeneath constitute the active regions, as is known to those of ordinary skill. Although the source and drain regions are not shown in Figure 2B, a source and a drain (active regions), a source and a drain (active regions) must exist in order to properly form a transistor. Therefore, the active region is located beneath the transistor gate structure, the active region being proximate to each of the resistor elements. Accordingly there is disclosure for active regions in the invention of Babcock.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J Sutton whose telephone number is 703-305-0070. The examiner can normally be reached on M-F 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

tjs
October 10, 2002

Carl Whitehead Jr.
CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800